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WASHBURN, DANIEL C	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/655,695	IOTOV, MIHAIL	
	Examiner	Art Unit	
	Dan Washburn	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _12 April 2007_.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1-20_ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _1-20_ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments filed 4/12/07 have been fully considered but they are not persuasive.

As to the applicant's argument that Pramanick fails to disclose, "displaying pointers to the time points of interest on the first and second waveforms; and receiving edits to the time points of interest in response to a user moving the pointers on the interactive graphical user interface." The examiner feels that this point is moot as Pramanick is not relied upon to describe the recited limitations.

As to the applicant's argument that Pramanick doesn't describe, "updating timing parameters based on the edits to the time points of interest," the examiner contests that while Pramanick doesn't disclose, "receiving edits to the time points of interest in response to a user moving the pointers on the interactive graphical user interface," Pramanick still discloses, "receiving edits to time points of interest" and "updating timing parameters based on edits to time points of interest," as is discussed in the rejection of claims 1, 2, and 11.

As to the applicant's argument that Alexander does not describe, "displaying pointers to time points of interest on the first and second waveforms," the examiner contests that Alexander teaches exactly this, as is discussed in the rejection of claims 1, 2, and 11.

As to the applicant's argument that Alexander does not describe, "receiving edits to the time points of interest in response to a user moving the pointers on the interactive

graphical user interface; and updating the timing parameters based on the edits to the time points of interest." The examiner feels that this point is moot as Alexander is not relied upon to describe the recited limitations.

As to the applicant's argument that Tojima doesn't describe, "displaying pointers to the time points of interest on the first and second waveforms; receiving edits to the time points of interest in response to a user moving the pointers on the interactive graphical user interface; and updating the timing parameters based on the edits to the time points of interest." The examiner contests that Alexander is relied upon to teach displaying multiple pointers to the time points of interest on the first and second waveforms (see the rejection of claims 1, 11, and 12 below), and Tojima describes displaying a single pointer to a time point of interest on the first and second waveform (column 18 lines 20-67 through column 19 lines 1-7 describe that displayed signal waveforms can be graphically edited. A user can place a mouse cursor on a particular waveform signal and then click and drag the mouse cursor in order to insert a delay at the beginning of the displayed waveform. A user can also place the mouse cursor on a particular waveform and double-click the left button on the mouse in order to invert the signal of the displayed waveform. The displayed mouse cursor is considered a pointer that a user uses to point to a time point of interest on either the first or second waveform);

receiving edits to the time points of interest in response to a user moving the pointers on the interactive graphical user interface (column 18 lines 30-51 describes that a user can insert a delay into a particular waveform by clicking and dragging a

mouse pointer when it is positioned on the waveform. A user clicking and dragging a mouse pointer on the graphical user interface in order to add a delay into the waveform diagram is considered the system receiving edits to the time points of interest (in this case a waveform of interest) in response to a user moving the pointer (in this case the mouse pointer) on the interactive graphical user interface); and

updating the timing parameters based on the edits to the time points of interest (column 18 lines 20-51 describes that when a user clicks and drags a waveform signal the process is stored as the circuit behavior "delay" in the database. Likewise, when a user double-clicks on a signal in order to invert it, the process is stored as the circuit behavior "invert whole signal" in the database. Column 18 lines 43-65 describes that the circuit behaviors stored in the database are extracted and are converted to functional element descriptions, which in this case translates to a flip-flop, in order to create the required delay, and an inverter, in order to invert the signal. The system storing the appropriate circuit behavior in the database as a result of the edits made to the displayed waveforms is considered updating the timing parameters based on the edits to the time points of interest).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2, 11, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pramanick et al. (US 2004/0216005) in view of Alexander (US 2002/0030683) and further in view of Tojima et al. (US 6,898,771).

As to claims 1, 2, and 11, Pramanick describes a method and computer readable medium for displaying timing data generated by simulating a circuit design, the method and computer readable medium comprising: receiving the timing data from an EDA tool (Figure 6 and paragraphs 0048-0050); selecting first and second signals based on input received from a user (paragraphs 0049-0050 describe that a user is able to create testbenches 73, 74, which select and test signals based on the user defined variables in the testbenches. The signals that are selected are considered to include at least first and second signals); generating a first waveform for the first signal and a second waveform for the second signal using the timing data (paragraph 0051 describes that event data from the EDA tool is passed to a GUI that displays waveforms of the actual test pattern (such as waveform image 91)); displaying a portion of each of the first and second waveforms in an interactive graphical user interface, wherein the portion of each of the first and second waveform displayed in the interface includes time points of interest to the user (paragraph 0051 describes that a user can select an area within overall waveform image 91 in order to generate an enlarged view 92 of a selected portion of the test pattern, which is considered to include time points of interest to a user); receiving edits to the time points of interest (paragraph 0051 describes offset image 93, in which the timing (or position) of specific edges are freely changed); and updating timing parameters based on the edits to the time points of interest (paragraph

0051 describes that changing in the parameters on the display can be done by modifying the event data in the event file 86, which also changes the actual test pattern applied to the device under test and thus enables the system and the user to monitor the resultant response of the device under test).

Pramanick doesn't describe displaying pointers to the time points of interest on the first and second waveforms.

However, Alexander describes a system and method of graphically annotating a waveform display in a signal-measurement system (paragraph 0018). Alexander further describes that the graphical annotations can include a graphical pointer or reference line, which enables the user to identify even a very small region of the displayed waveform (paragraph 0107). Paragraph 0109 describes the specific process of adding an annotation label to the display. The process describes that a user places a mouse cursor at a specific position on the graph, clicks the right button on the mouse, and then selects "add label" to create a new label. The mouse cursor is considered a first type of pointer that is used to point to a time point of interest on the first or second waveform and the annotation label (which includes a graphical pointer) is considered a second type of pointer that is also used to point to a time point of interest on the first or second waveform. It would have been obvious to one of ordinary skill in the art at the time of the invention to include in Pramanick the system and method of displaying pointers to time points of interest on the waveform, as taught by Alexander, in order to allow the user to add descriptions to the waveform describing various transitions or signal states, and further to allow the user to identify very small regions on the waveform using the

disclosed graphical pointers. The advantage of the user adding graphical pointers to the waveforms is that the user is able to create notes on the waveform, which is helpful when trying to remember why saved waveform diagrams are important, or when trying to explain problems using the waveform diagrams.

Pramanick in view of Alexander doesn't describe receiving edits to the time points of interest in response to a user moving the pointers on the interactive graphical display interface.

However, Pramanick does describe that a user can use offset image 93 to alter the timing (or position) of specific edges found within the waveform, where the user alters the parameters by modifying the event data in the event file 86 (paragraph 0051).

Further, Tojima describes a system and method of designing a semiconductor integrated circuit device where a user is able to modify timing diagrams and the system will automatically generate the necessary logic between or within circuit blocks to implement the change in circuit behavior (column 2 lines 16-40). Tojima also offers Figure 13A, which is a timing chart illustrating a method of modifying a signal waveform. Figure 13A illustrates that signal B can be delayed two clock cycles if a user clicks and drags the waveform, or signal B can be inverted, if a user double-clicks on a waveform. This change in the timing diagram is translated into a functional element, such as a flip-flop or an inverter, and the change is made in hardware to reflect the change in the timing diagram (column 18 lines 20-67 and column 19 lines 1-40). In the description offered in Tojima a user uses the mouse cursor displayed on the screen to edit certain points on a waveform (e.g., delay the signal or invert the signal). The mouse cursor is

considered a pointer on the interactive graphical display interface. It would have been obvious to one of ordinary skill in the art at the time of the invention to include in Pramanick in view of Alexander the system and method of receiving edits to the time points of interest in response to a user modifying certain points on a waveform (and, given the disclosure of pointers as taught by Alexander, the corresponding graphical pointers) using the mouse cursor pointer on a graphical interactive display interface, as taught by Tojima, in order to make the process of altering a waveform (considered editing time points of interest) even easier by allowing a user to directly alter the displayed waveforms, rather than only allowing a user to alter an associated event file, as taught in Pramanick. The advantage of allowing a user to directly alter the waveform in order to implement changes to the timing of the integrated circuit is that complicated functions, such as delaying or inverting a signal, can be easily carried out with little to no knowledge as to the underlying variables that were actually altered; thus, the program is more user-friendly.

(Regarding claim 2 and the remaining limitations of claim 11) Pramanick further describes a method and computer readable medium comprising; transmitting the updated timing parameters back to the EDA tool (paragraphs 0049-0050 and Figure 6 describe that through a logic simulation process a dump file (VCD) 78 is produced. The dump file is passed to an interface 81 in order to produce an event file 86. The event file is altered by a user (paragraph 0051), and test system hardware 88 generates a test result file 76, which is passed back to the EDA tool through testbench generator 75); generating updated first and second waveforms for the first and second signals using

updated timing data received from the EDA tool, wherein the updating timing data is generated by simulating the circuit design using the updated timing parameters (Figure 6 and paragraphs 0050-0051 describe that the process of running a circuit simulation, generating waveforms, altering the waveforms, and running a new circuit simulation based on the altered waveforms is circular, where the new circuit simulation generates updated waveforms for the relevant signals using the updated timing parameters); and displaying the updated first and second waveforms in the interactive graphical user interface (paragraph 0051 and Figure 6 describe that waveforms are displayed through a GUI).

Concerning claim 12, Pramanick describes a computer readable medium wherein the display of the portion of each of the waveforms in the interactive graphical user interface further comprises display of each of the portions of the waveforms in synchronism (Figure 6 and paragraph 0051 describes waveforms images 91, 92, 94, and 95, which are all displayed through a GUI and each is considered an image that displays waveforms in synchronism, as more than one waveform is displayed on each image).

Claims 3-10 and 13-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pramanick et al. (US 2004/0216005) in view of Alexander (US 2002/0030683) and further in view of Tojima et al. (US 6,898,771), as applied to claims 1 and 11 above, and further in view of Liu et al. (US 6,662,126).

With regard to claims 3 and 14, the combination of Pramanick, Alexander, and Tojima doesn't describe a method or computer readable medium wherein displaying the

portion of each of the first and second waveforms in the interactive graphical user interface further comprises displaying a first waveform of a first clock signal received at a first storage element, and a second waveform of a second clock signal received at a second storage element.

However, Liu describes a system and method of measuring signal skew on a chip using on-chip sampling. Each on-chip sampler takes in an external signal and a global on-chip signal, and the samplers are compared to determine how much signal skew occurs as the signals propagate from one portion of the chip to a second portion of the chip (Figure 3 and column 3 lines 11-37). Further, Liu offers Figure 6, which illustrates a timing diagram that describes how the skew of a global on-chip signal between two different points can be determined by using on-chip samplers. Figure 6 illustrates a first external modulated signal MOD_EXT_1 at a first point on the chip, an on-chip signal at the first point, CHIP_CLK_1, the same modulated signal at a second point on the chip, MOD_EXT_2, and the same on-chip signal at the second point, CHIP_CLK_2. The difference between these two signals, and the difference between both of these signals and the original input signals, describes a measurable amount of signal skew that occurs as a clock signal and an external signal propagate through the chip (column 7 lines 61-67 and column 8 lines 1-22). The on-chip samplers are described as being made up of transistors and inverters (column 4 lines 27-31), therefore the on-chip samplers are considered storage elements. It would have been obvious to one of ordinary skill in the art at the time of the invention to include in Pramanick, Alexander, and Tojima the system and method of measuring a first

waveform of a first clock signal received at a first storage element, and a second waveform of a second clock signal received at a second storage element, as taught by Liu, and displaying these measured waveforms on the interactive graphical user interface described by Pramanick, Alexander, and Tojima, in order to allow a user to alter the timing of certain logical operations on the chip using the actual waveforms that the storage elements receive at their inputs, rather than the ideal clock waveform that doesn't account for signal skew. The advantage of allowing a user to work with the actual signals that each storage device receives at its input is that a user can fine tune the circuit timing to a very precise level, as he can adjust for signal skew and other factors that can't be compensated for when working with an ideal clock signal.

As to claims 4 and 15, the combination of Pramanick, Alexander, and Tojima doesn't describe a computer readable medium or method wherein displaying the portion of each of the first and second waveforms in the interactive graphical user interface further comprises displaying a third waveform of the first clock signal at first clock source, and a fourth waveform of the second clock signal at a second clock source, the first waveform of the first clock signal being delayed with respect to the third waveform by a first clock skew value, and the second waveform of the second clock signal being delayed with respect to the fourth waveform by a second clock skew value.

However, Liu describes a system and method of measuring the clock skew of an on-chip clock signal using an external signal and the global on-chip clock signal (column 3 lines 11-27, column 7 lines 61-67, and column 8 lines 1-22). Figure 3 illustrates two externally input signals, EXT and CHIP_CLK, and Figure 6 illustrates the signals as they

appear at a first on-chip sampler (MOD_EXT_1, CHIP_CLK_1) and a second on-chip sampler (MOD_EXT_2, CHIP_CLK_2). It would have been obvious to one of ordinary skill in the art at the time of the invention to include in Pramanick, Alexander, and Tojima the system and method of measuring a waveform (considered a third waveform) of a first clock signal at a first source (EXT is considered a first clock signal), and measuring a waveform (considered a fourth waveform) of a second clock signal at a second source (CHIP_CLK is considered a second clock signal), where the first waveform (in this case MOD_EXT_1 or MOD_EXT_2) is delayed with respect to the third waveform by a first clock skew value, and the second waveform (in this case CHIP_CLK_1 or CHIP_CLK_2) is delayed with respect to the fourth waveform by a second clock skew value, as taught by Liu, and displaying these measured waveforms on the interactive graphical user interface described by Pramanick, Alexander, and Tojima, in order to allow the user to see exactly the extent of the signal skew that exists between the originally input signals and various points within a chip. The advantage of displaying the original signals along with the skewed signals is that a user can easily determine if the signal skew is unacceptably large at certain points on the chip and alter the design in order to correct the problem. Measuring and displaying signal skew allows a user to fine tune the circuit timing to a very precise level, as he can adjust for signal skew and other factors that can't be compensated for when working with an ideal clock signal.

Concerning claim 5, Pramanick describes a method wherein displaying the portion of each of the first and second waveforms in the interactive graphical user

interface comprises displaying a launch edge of the first clock signal at which the first storage element releases a data signal, and displaying a latch edge of the second clock signal at which the second storage element captures the data signal (Figures 4B and 5A-5C and paragraphs 0043-0046 describe two flip-flops and their associated timing diagrams. Figure 5A illustrates that the input of the first flip-flop is driven high at 61, then at clk2 the input is latched into the first flip-flop (signal b at arrow 62), there is a bit of a propagation delay due to gate logic between the two flip-flops, and then the signal shows up at the input to the second flip-flop (signal c) and it is latched into the second flip-flop at clk3 (arrow 64). Signal b at arrow 62 is considered the launch edge of the first clock signal at which the first storage element releases a data signal, and signal d at arrow 64 is considered the latch edge of the second clock signal at which the second storage element captures the data signal. These waveforms are presented to the user using the system described in Figure 6).

With regard to claim 6, Pramanick describes a method wherein the interactive graphical user interface displays portions of the first waveform of the first clock signal and the second waveform of the second clock signal that each start with a point in time corresponding to a period before both the launch and latch edges and end with a point in time corresponding to a period following both of those edges (Figures 5A-5C all illustrate portions of the first and second waveforms that each start with clk1, which is considered at point in time corresponding to a period before both the launch and latch edges, and end at clk4 or unlabeled clk5 (the clock cycle after clk4) which is a point in time corresponding to a period following both of those edges).

As to claims 7, 16, and 17, Pramanick doesn't describe a method or a computer readable medium wherein the launch edge is a first time point of interest identified by a first one of the pointers on the interactive graphical user interface; and the latch edge corresponds to a second time point of interest identified by a second one of the pointers on the graphical user interface, nor does he describe code for displaying a first pointer to a launch edge of the first waveform that triggers a first latch to capture a data signal; code for displaying a second pointer to a latch edge of the waveform that triggers a second latch to capture the data signal; code for displaying a third pointer to an edge of the third waveform that corresponds to the launch edge of the first waveform; and code for displaying a fourth pointer to an edge of the fourth waveform that corresponds to the latch edge of the second waveform.

However, Alexander describes a system and method of graphically annotating waveforms using pointers and text boxes (paragraph 0018 and 0107). It would have been obvious to one of ordinary skill in the art at the time of the invention to include in Pramanick the system and method of identifying a trigger for a launch edge and an actual launch edge of one storage element and a trigger for a latch edge and an actual latch edge of a second storage element using pointers, as taught by Alexander. See the rejection of claim 1 for motivation to combine Alexander with Pramanick, as the same motivation applies here.

Regarding claim 8, Pramanick describes a method wherein updating the timing parameters based on the edits to the time points of interest further comprises updating a multi-cycle value that represents a number of active edges in the second clock signal

between the launch edge and the latch edge (Figures 5B and 5C and paragraphs 0044-0046 describe that a user is able to alter the timing of the clock (considered a second clock signal) that two flip-flops operate off of in order to correct a timing error. In Figure 5B the propagation delay (delta bc2) between the launch edge of a first flip-flop and the latch edge of a second flip-flop is so large that a clock cycle passes before the value is ready to be latched by the second flip-flop. The logic that takes place between these two flip-flop operations is considered to have a multi-cycle value of one, as there is one active (positive) edge in the clock signal between the launch edge and the latch edge. A problem occurs at this point because the second flip-flop attempts to latch the incoming value at clk3, but the value isn't ready, so the second flip-flop latches an incorrect value. In order to remedy this problem a user is able to alter the timing parameters of the clock during the propagation delay in order increase the period of the clock. The increased clock period gives the launch edge from the first flip-flop enough time to propagate through the required logic and arrive at the input of the second flip-flop before the next positive edge of the clock, which corrects the timing error. The multi-cycle value that represents a number of active edges in the clock signal between the launch edge and the latch edge has been updated from one to zero, as now there are zero active edges in the clock between the launch edge and the latch edge).

Concerning claims 9 and 10, Pramanick in view of Alexander doesn't describe a method wherein updating the timing parameters based on the edits to the time points of interest further comprises inverting the launch edge of the first clock signal, either in a design file or as an input to a static timing verification tool, nor does the combination

describe a method wherein updating the timing parameters based on the edits to the time points of interest further comprises inverting the latch edge of the second clock signal.

However, Tojima describes a method wherein updating the timing parameters based on edits to the time points of interest further comprises inverting displayed waveforms, which is considered to include inverting the logic that controls the launch edge and latch edge for storage devices (Figures 13A and 13B and column 18 lines 20-51 describes that a user may double-click on a waveform in order to invert the entire signal). It would have been obvious to one of ordinary skill in the art at the time of the invention to include in Pramanick in view of Alexander the method of inverting the launch edge of a clock signal and inverting the latch edge of a clock signal, as taught by Tojima, in order to test the performance of a circuit using negative logic, where the flip-flops launch and latch values based on the negative edges of a clock signal. The advantage of testing a circuit using negative logic is that a user can see how the circuit reacts to a wider range of tests, which helps create a more robust design.

With regard to claim 13, Pramanick describes a computer readable medium wherein the timing data generated by the EDA tool includes the period of a clock signal and the duty cycle of a clock signal (Figure 6 and paragraphs 0048-0049 describe that the EDA environment generates a dump file 78 as a result of a logic simulation process 72 that is applied to LSI data 71. This information is passed to the event based test system interface 81, which eventually results in an event file 86. The event file 86 is what is used to generate waveform images 91-95, which includes a displayed period of

a clock signal used and a displayed duty cycle of a clock signal used (see Figures 5A-5C).

The combination of Pramanick, Alexander, and Tojima doesn't describe that the timing data generated includes a plurality of clock signals, duty cycles for a plurality of clock signals, offsets between the clock signals, and clock skews between sources of the clock signals and circuit elements that receive the clock signals.

However, Liu describes a computer readable medium that measures periods of a plurality of clock signals (EXT and CHIP_CLK, of Figure 3 are considered clock signals), duty cycles of clock signals (Figure 6 illustrates the measured clock signals at a first and second on-chip sampler, which includes the duty cycles of the measured clock signals), offsets between the clock signals, and clock skews between sources of the clock signals and circuit elements that receive the clock signals (Figure 6 illustrates MOD_EXT_1, CHIP_CLK_1, MOD_EXT_2, and CHIP_CLK_2, which are clock signals received at a first and second on-chip sampler, respectively, are offset from each other and from the original clock inputs, and are skewed signals with respect to each other and with respect to the original clock inputs (column 7 lines 61-67 and column 8 lines 1-22)). It would have been obvious to one of ordinary skill in the art at the time of the invention to include in Pramanick, Alexander, and Tojima the system of generating timing data that includes periods of clock signals, duty cycles of clock signals, offsets between the clock signals, and clock skews between sources of the clock signals and circuit elements that receive the clock signals, as taught by Liu. See the rejection of

claims 3, 4, 14, and 15 for motivation to combine Liu with Pramanick, Alexander, and Tojima, as the same motivation applies here.

As to claims 18 and 19, Pramanick describes a computer readable medium wherein the code for generating the new timing parameters based on the edits to the time points of interest further comprises code for changing a multi-cycle value that represents a number of active edges in the second clock signal from the launch edge to the latch edge, as described in the rejection of claim 8.

Pramanick doesn't describe a first, second, third, and fourth pointer on the graphical user interface.

However, Alexander describes a system and method of graphically annotating waveforms using pointers and text boxes (paragraph 0018 and 0107). It would have been obvious to one of ordinary skill in the art at the time of the invention to include in Pramanick the system and method of including a first, second, third, and fourth pointer on the graphical user interface, as taught by Alexander. See the rejection of claim 1 for motivation to combine Alexander with Pramanick, as the same motivation applies here.

Pramanick in view of Alexander doesn't describe that the system of changing a multi-cycle value that represents a number of active edges in the second clock signal from the launch edge to the latch edge is in response to a user moving the first, second, third, or fourth pointer on the graphical user interface.

However, Tojima describes a system and method of designing a semiconductor integrated circuit device where a user is able to modify timing diagrams and the system will automatically generate the necessary logic between or within circuit blocks to

implement the change in circuit behavior (column 2 lines 16-40). Tojima also offers Figure 13A, which is a timing chart illustrating a method of modifying a signal waveform. Figure 13A illustrates that signal B can be delayed two clock cycles if a user clicks and drags the waveform, or signal B can be inverted, if a user double-clicks on a waveform. This change in the timing diagram is translated into a functional element, such as a flip-flop or an inverter, and the change is made in hardware to reflect the change in the timing diagram (column 18 lines 20-67 and column 19 lines 1-40). In the description offered in Tojima a user uses the mouse cursor displayed on the screen to edit certain points on a waveform (e.g., delay the signal or invert the signal). The mouse cursor is considered a pointer on the interactive graphical display interface. It would have been obvious to one of ordinary skill in the art at the time of the invention to include in Pramanick in view of Alexander the system and method of receiving edits to the time points of interest, and specifically for changing a multi-cycle value that represents a number of active edges in the second clock signal from the launch edge to the latch edge, in response to a user modifying certain points on a displayed waveform (and, given the disclosure of pointers as taught by Alexander, the corresponding graphical pointers) using the mouse cursor pointer on a graphical interactive display interface, as taught by Tojima, in order to make the process of altering a waveform (considered editing time points of interest) even easier by allowing a user to directly alter the displayed waveforms, rather than only allowing a user to alter an associated event file, as taught in Pramanick.. See the rejection of claims 1 and 11 for motivation to combine Tojima with Pramanick and Alexander, as the same motivation applies here.

Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Pramanick et al. (US 2004/0216005) in view of Alexander (US 2002/0030683) and further in view of Tojima et al. (US 6,898,771), as applied to claims 1 and 11 above, and further in view of Chan (US 6,466,898).

The combination of Pramanick, Alexander, and Tojima doesn't describe a computer readable medium wherein the circuit design is a design for a field programmable gate array.

However, the background of Chan describes that a logic simulator is an essential electronic design automation (EDA) tool to facilitate the design and debug of very large scale integrated circuits (column 1 lines 5-20). The background of Chan further describes that some EDA vendors have hardware-accelerators or hardware emulators, where the hardware emulators program field programmable gate array (FPGA) chips (column 2 lines 4-23). It would have been obvious to one of ordinary skill in the art at the time of the invention to include in Pramanick, Alexander, and Tojima the system of using the EDA tool and timing analyzer to program an FPGA, as taught by the background of Chan, in order to apply the system taught by Pramanick, Alexander, and Tojima to debugging and programming FPGA chips, which increases the market demand for the system, as an FPGA chip is a common and popular chip to work with for commercial and educational purposes.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Washburn whose telephone number is (571) 272-5551. The examiner can normally be reached on Monday through Friday 8:30 a.m. to 5:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ulka Chauhan can be reached on (571) 272-7782. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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6/26/07

Ulka Chauhan
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